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A study of a data acquisition and reduction system

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A STUDY OF A DATA ACQUISITION AND REDUCTION SYSTEM

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ABSTRACT

This paper describes a system that tests magnetic memories, digitalizes the sampled memory output, stores the data on magnetic tape, and reduces the data to usable form. A buffer memory is used to compensate for the speed differential between the memory test set and the magnetic tape unit. All the equipment and necessary interfacing is described. Designs for circuits to add parity and check parity, and a console unit are presented to complete the system layout.

A STUDY OF A DATA ACQUISITION AND REDUCTION SYSTEM

Introduction

The field of memory devices is broad, active, and constantly expanding. The types of memory cells have evolved from the simple ferrite toroid to the ferrite sheet, to various types of fluxors and transfluxors, the twistor and its ramifications, and more recently to thin films and cryogenic elements. The accent is on higher capacity, higher speeds, and lower costs. On the other hand, techniques for testing these devices have lagged the field considerably.

Precise techniques for testing the memory cells themselves have been developed and are reasonably simple and straightforward. The test for a memory, however, has been "does it work in the store[1]?" This author feels that such an approach is intrinsically wrong and inadequate. Due to the complex nature of a store, it is impossible to tell whether the memory is under test, the store is under test, or some combination of both is under test. Furthermore, one can never really know the character of a memory device with this approach, but merely some of its attributes. Go, no-go memory testing is certainly not wrong from a production standpoint, provided

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[1]The term "store" refers to a memory system composed of a memory and associated access circuitry.

the test conditions are known and understood. But surely the designer in the laboratory should have more information in order to improve and expand the present design and to create new designs.

Satisfactory operation of a memory cell does by no means guarantee satisfactory operation of the memory in which it is used. Some of the variables to be considered are delta noise, wiring patterns, and the transmission line effect of readout wires. For the most part these variables are incalculable and must be evaluated by experimentation. In order to get a thorough understanding of the effects of these variables, vast accumulations of data are required. The purpose of this paper is to outline a method of acquiring this data and reducing it to usable form.

General Approach

When one considers going through a 200,000 bit memory several times under varying conditions in an attempt to assess the data that comes from the memory, he soon realizes that a computer must be the end block of his system, otherwise he would be faced with so much data the analysis problem would be insurmountable.

Another consideration is that of getting the data to the computer. The most convenient and economical

method to do this appears to be magnetic tape. If the acquisition time of the test set from which the data is to be obtained is less than the time necessary to write on magnetic tape, the tape unit could control the test set directly and call for the information at its own speed. In the event that the tape unit is much faster than the test set, a buffer memory would have to be used as an interface between the two units. The second case, since it is the more general, will be considered here. The data flow of this simple system as it now appears starts from a test set, goes into a buffer memory, onto magnetic tape, and into the computer for reduction.

Before going into a detailed analysis of the problem, it should be stated here that this is not a hypothetical or academic problem, but one that is under consideration at this time. It should further be noted that the actual test set to be used as the first block of the system is in existence. Therefore, a brief description of the test set is in order.

Memory Test Set Capabilities

The test set is capable of sequentially scanning coincident current memory modules as large as 16,384 words, 48 bits per word with address to address cycling speed presently limited by dry-reed-relay access switches to 5 milliseconds. A stepping switch connects three adjacent

module inhibit windings to three inhibit drivers. Another other stepping switch synchronized with the inhibit stepping switch connects the module sense winding associated with the middle of the three selected inhibit windings to the readout circuitry. A write program generator which controls the inhibit drivers is programmed by a toggle switch matrix. This write program generator enables the machine to store various information patterns along three adjacent sense windings as the module is scanned. After a preset number of scanning cycles (scanning cycle defined as one complete pass through the memory by sequential addressing along one bit plane) with the readout circuit connected to a particular sense winding, a signal is produced which advances the stepping switches to select the next sense and inhibit windings. The scanning sequence is then repeated. This process continues until the last sense winding in the module has been selected. It is also possible to program the entire memory module but test only particular segments. A circuit is available which activates the output circuit during portions of the scanning cycle determined by addresses preset on a toggle switch panel.

To take advantage of this program flexibility and in order to identify each bit as it comes from memory, program information must accompany each bit. Voltage

amplitudes expected from the memory range from several millivolts to over a hundred millivolts. These voltages, of course, must be encoded in digital form before they go on tape.

Detailed Approach

Several computers were available to do the data reduction. The IBM 7090 computer was chosen to do the job because of its cost-speed advantage. Before going into the input requirements for the computer, several other aspects of the system will be considered.

The first consideration is the kind of information we want to get from the test machine. For each cell under test we want to know the amplitude of the bit; if the bit is a "one" or a "zero," this we will call a telzyu bit; a sign bit; and the program position. The amplitude will require six bits; the telzye bit, one bit; the sign bit, one bit; and the program position, four bits. These twelve bits are treated as two six bit words with a parity bit added to each word for a total of fourteen bits required to describe each bit out of the memory under test. In order to minimize the capacity of the buffer store, relatively small sized blocks of information will be taken from the test set, put into buffer and then dumped onto tape, thereby clearing the buffer for more storage. Treating the information as blocks, that is, not going through the entire memory sequentially can be turned to advantage as long as each block is identified. By maintaining the information within each block

in sequential order, each block can be completely identified by a heading comprised of a starting address, a bit wire number, and an end of block word.

System Operating Sequence

The general system operation sequence is as follows. The first information that goes onto the tape is a general heading which identifies the memory and the conditions under which it is being tested. This information goes on from the console keyboard, Figure I, and is put in manually in binary form in six bit bytes. In this system a byte is limited by the tape width, which is six bits plus one parity bit wide. Each byte is gated into the input register of the buffer manually and then gated into buffer storage automatically after which the buffer address counter is advanced one count. When the heading information has been completed, that is, entirely in buffer storage, an end of block word is added and the tape transport is given control of the buffer store to extract this information from the buffer and put it on tape. Again this operation occurs in six bit (plus parity) bytes. Each byte is parity checked before going on tape. When the tape unit has the entire heading, it checks vertical parity, which detects tape errors, and raises a flag if there is no check. If the vertical parity checks, the system is reset, the buffer is cleared and waits for the test set to put out the first block of information. A block of data

is put on tape in the following manner:

1. a. The first bit from the memory under test is addressed and read out. The readout is then fed into the sample and hold circuit. This circuit takes a narrow sample of the amplitude, stretches it out in time, and feeds it into the analog-to-digital converter which encodes the signal into six bits. A parity bit is then added to the initial six bits and the seven bits set on the output register of the converter. The converter also generates the sign bit which indicates whether the output of the memory under test was positive or negative. This sign bit, four program bits and one telzyu bit are fed into the add parity circuit, become parity encoded and exist there as levels.

b. The A/D converter now gates all fourteen bits into the input register of the buffer. The fourteen bits are then gated into the buffer memory to an address that corresponds to the address of the bit from the memory under the test.

c. The analog-to-digital converter and the sample and hold circuit are cleared, and the address register of the buffer store is advanced one count.

2. Sequences 1.a through 1.c are repeated until the last bit from the memory under test in the block is in the buffer store. An end of block word is generated by the test set and stored in the buffer.

3. The test set now releases control of the buffer store and informs the tape transport that a block of information is in the buffer.
4. The tape transport assumes control of the buffer, starts its reels, and tells the buffer to send in bits one through seven of the first word which is fourteen bits in length.
5. Bits one through seven are parity checked and then put onto tape.
6. The tape transport tells the buffer to send in bits eight through fourteen of the first word.
7. Bits eight through fourteen are then parity checked and also put onto tape.
8. The tape transport tells the buffer to send in bits one through seven of the second word, etc.
9. When the last word in the buffer has been put on tape, this would be the end of block word. The tape transport stops its reels.
10. The transport releases control, the entire system is reset and awaits the next block heading information to come from the console.

Sample and Hold Circuit

The discrimination ratio, i.e., the amplitude of a "one" signal to the amplitude of a "zero" ratio is not only a function of maximum amplitudes but also of time.

Consequently, the memory output is always strobed. In order to obtain high precision in the amplitude--time measurement, a sampler with a variable strobe position and a sample width of about one nanosecond is being developed. The sample is then stretched or "held" for about twenty microseconds--long enough to be amplitude encoded by the analog-to-digital converter.

The present state of development of this circuit indicates that there must be a KEEP ALIVE clock feeding the unit during its inactive period. The KEEP ALIVE function may be supplied by the test set. As long as the circuit is in operation this function is unnecessary.

Analog-To-Digital Converter

When presented with an analog voltage of at least fifteen microseconds duration, the converter digitalizes the analog into six information bits and adds one parity bit. It also determines the sign of the analog input and relays this information to the ADD PARITY CIRCUIT as one bit. The A/D converter supplies a pulse that gates the data from its output register and the information from the ADD PARITY CIRCUIT into the buffer input register. This same pulse then causes the buffer to store the data and advance the address register.

Add Parity Circuit

This circuit consists of five transformers, ten diodes and a parity flip-flop, Figure 2. The transformer and diodes form five "exclusive or" circuits. The opera-

tion of one such "or" circuit is as follows:

Consider the transformer T_1, its diodes, and the upper primary of T_4. If inputs A and B are both present, there will be no induced voltage in the secondary due to the bucking action. If either A or B is present, there will be a secondary current that flows through only one of the diodes and the upper half of the T_4 primary, thereby accomplishing the "exclusive or" function.

The over-all operation is such that inputs A-F are simultaneously gated into the ADD PARITY circuit. If the number of inputs that are up is odd, the parity flip-flop will be triggered. Odd or even parity may be obtained by the choice of flip-flop outputs.

A delay problem may exist between T_3 and T_5. This can be rectified by either a proper delay line or a transformer similar to T_4.

Console

The console performs two major functions. It must be able to add heading information to each block of information and have control over the tape unit. The main interest here is in the former since the latter function can be part of the tape control unit specification.

Figure 4 shows one way to add heading information. The six data switches, S1-S6, are the manual input switches

that set up paths from the monopulser to the ADD PARITY circuit. Indicator lights are lit on the console when binary ones are loaded into the parity circuit. S7 triggers the monopulser. The information set up on switches S1 through S6 becomes parity encoded and exists at the inputs to "AND" gates, A through P, as long as the monopulser is on. Meanwhile the output of the monopulser is delayed through D1, long enough for the parity flip-flop to become "set." The data bits plus parity are then ANDed through the first set of gates into "AND" gates one through seven, or eight through fourteen depending on the state of the complimentary flip-flop, FF1. The outputs of these gates are ORed with the output of the fourteen gates associated with the A/D converter and ADD PARITY circuits that handle data. At this point the logic level is -3 volts and must be changed to +5 volts at the input to the buffer register.

While the information is being put in the buffer register, the monopulser output is again delayed by D2, used to reset the parity flip-flop, inverted to +5 volts and counted by FF2. There is no output at this point when bits one through seven are loaded into the buffer register. However, when bits eight through fourteen are loaded, FF_2 produces a signal that writes the contents of the buffer register into memory after which the buffer address counter advances one count.

When all the heading information is loaded in buffer storage, the tape control unit takes control of the buffer and enters its contents on tape. If, during this operation a parity check error occurs, a trouble lamp is lit on the console by the FALSE WORD circuit. Since a false word in heading information cannot be tolerated, the operator must repeat the tape dump cycle until no errors are indicated.

Buffer

The buffer store to be used in the system is an in-house item with a storage capacity of 8,192 words, 24 bits per word. It operates at a read-write cycle time of 5.5 microseconds. During the tape dump cycle, the information in storage is called for by the tape unit, written on tape, then restored in the same memory location. The restoration or rewrite is done automatically. This is essential for proper operation of the system in that the data must be preserved until vertical tape parity has checked since no check means erroneous information has been put on tape. This point is pursued further in the section on the tape transport.

The buffer unit will have a duplicate counter which is set to the number of words that are in storage. The counter is then decremented by one as each word is read

out onto tape. When the counter reaches zero, the tape control unit receives a STOP TAKING DATA signal.

Shift Circuit

When the tape control unit requests a data word (fourteen bits) from the buffer, the entire word is read out of memory and exists as levels in the buffer output register. Each of the outputs of the register is connected to an input of a two input "and" gate. The output of gates one and eight are ORed at point A of the PARITY CHECK circuit; gates two and nine are ORed at point B, etc. To call for bits one through seven of a word, the tape control unit must generate a gate pulse that is fed to the other inputs of the two input "and" gates one through seven. Bits eight through fourteen are selected in a like manner.

Check Parity Circuit

Essentially the same circuit that adds parity may be used to check parity, Figure 3. If parity checks, all seven bits are gated to the tape unit. When parity does not check, a false word is gated to the tape unit.

The purpose of a false word is to provide information at that position on the tape normally occupied by data. The computer will know that the word is not data and treat it accordingly. Furthermore, since the data is sequential within a block, there must be something on the tape that the computer can "count" so as not to lose its place in the data block.

False Word Circuit

The false word must be seven bits in length and of a combination that the computer will recognize as being false, for instance perhaps 1100001. On the assumption that this is the false word, the circuit operates in the following manner (see Figure 5):

After the parity check flip-flop has made its decision, the tape control unit sends out a pulse that is ANDed with the "yes" side of the flip-flop. If the decision was "yes," the seven bits are gated to the tape input register. If the decision was "no," this side of the flip-flop is ORed to the tape input register on tape channels one, two, and seven, thereby establishing the false word 1100001. For a "no" condition a signal is also sent to the console indicator mainly to protect against false words appearing in heading information. The entire system is presented in more detail in Figure 6.

Data Reduction

As previously mentioned the reduction vehicle is to be the IBM 7090 computer. The detailed information desired has not yet been worked out, but a procedure for acquiring reduced data has been discussed with computer programming people.

It is felt that a very general and very complex program can be written that will include most conceivable

contingencies. Some of the desired data are: lowest 20 ones along with the conditions under which they were obtained; highest 20 zeros along with the conditions under which they were obtained; mean and standard deviation of all the data; and the distribution of corner hole outputs of ferrite sheet memories. Contingencies could occur in the following manner. The normal data presented to the computer may be the output of a 2,048 word, 24 bits per word, memory taken in one bit line blocks in complementary fashion. The data per bit line and the bit lines chosen by the test set would be in sequential form. Since such a format would, by definition, be called normal, complicated block heading information need not be entered because the program would recognize the data as being sequential. If, on the other hand, one wished to skip over a few bit lines and test, he must so indicate in the block heading so the computer will know how to treat the "misplaced" data.

Tape Transport and Tape Control Unit

The tape transport specification and capability are listed below:

Tape Speed:	112.5 inches per second, bi-directional
Start Time:	3 milliseconds
Stop Time:	2 milliseconds
Inter-Record Gap:	3/4 inch (IBM standard)
Stop Distance:	0.15 inch
Tape:	1/2 inch wide IBM std.-length up to 2,500 ft.
Rewind:	225 inches per second
Head:	7 channel read-after-write IBM compatible
Status Signals:	Low tape Tape being loaded End of tape Low point

The tape control unit must be capable of performing the following functions.

On tape parity error, the tape must back up to the beginning of the block and rewrite the entire block. If this occurs three times successively, that portion of the tape must be erased and rewritten in an advanced location. If this occurs three times, the entire system should stop and indicate the type of error that caused the system to stop.

The signals that the tape control unit must generate are as follows:

Reset buffer at end of block:	+5 volt level
Tape parity error-reset buffer:	+5 volt level
Tape dump timing:	+5 volt pulses
Shift to bits 1-7 out of buffer:	+5 volt pulses
Shift to bits 8-14 out of buffer:	+5 volt pulses
Reset parity check flip-flop:	+5 volt pulses
Strobe parity check flip-flop:	+5 volt pulses

The signals that the tape control unit must respond to are as follows:

Input data:	+5 volt level
End of block (from buffer):	+5 volt level
Stop taking data:	+5 volt level
Remote signals:	rewrite heading
	erase heading and advance beyond bad space
	rewind
	power on-off
	stop

Level Changes

The final compatability problem lies in the difference in logic levels between some of the units in the system. The following level changes must be introduced:

End of block-wait (from buffer to test set)	- change from +5 volts to -3 volts
Store	- change from -3 volts to +5 volts
Fourteen inputs to buffer register	- change from -3 volts to +4 volts
Store (from console to buffer)	- change from -3 volts to +5 volts

Conclusions

The system described herein, although apparently practical, is highly dependent on the tape control unit. A control unit to provide the necessary functions could undoubtedly be designed, but there may be a system cost penalty. A close liaison with control unit designers would resolve this point and may lead to some logic changes in the system that would result in an over-all cost saving.

Another vague area is that of programming the IBM 7090 computer. Although professional programmers have expressed assurance that it is a relatively straightforward matter to write a completely general program--one that would do the desired data reduction for all existing memories and most foreseeable ones, the author feels that more study is required before a definite commitment is made.

The cost of computer time on the 7090 is $650 per hour. The cost of time on the Honeywell 400 is only $60 per hour. However, the difference in processing time is such that the cost of processing 1,000 bits on the 7090 is $.007 compared to $012 on the Honeywell 400.

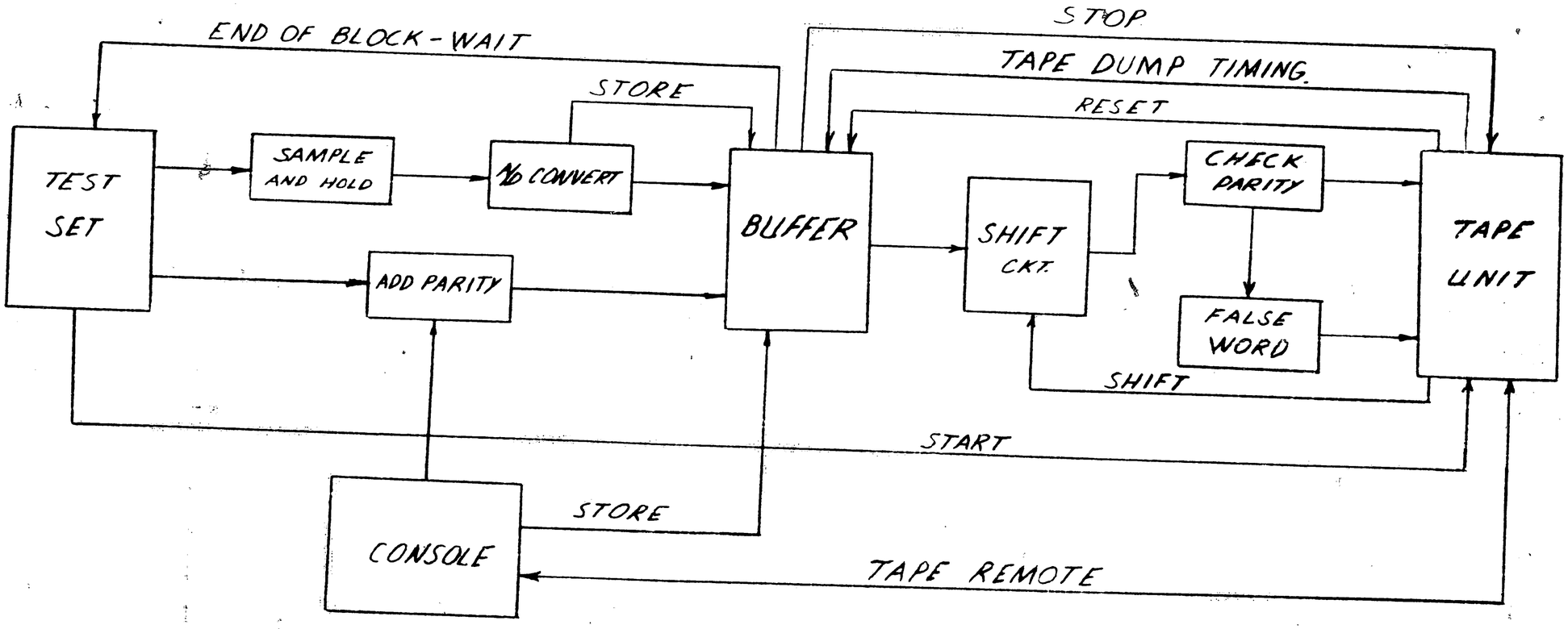

FIGURE 1 - BLOCK DIAGRAM

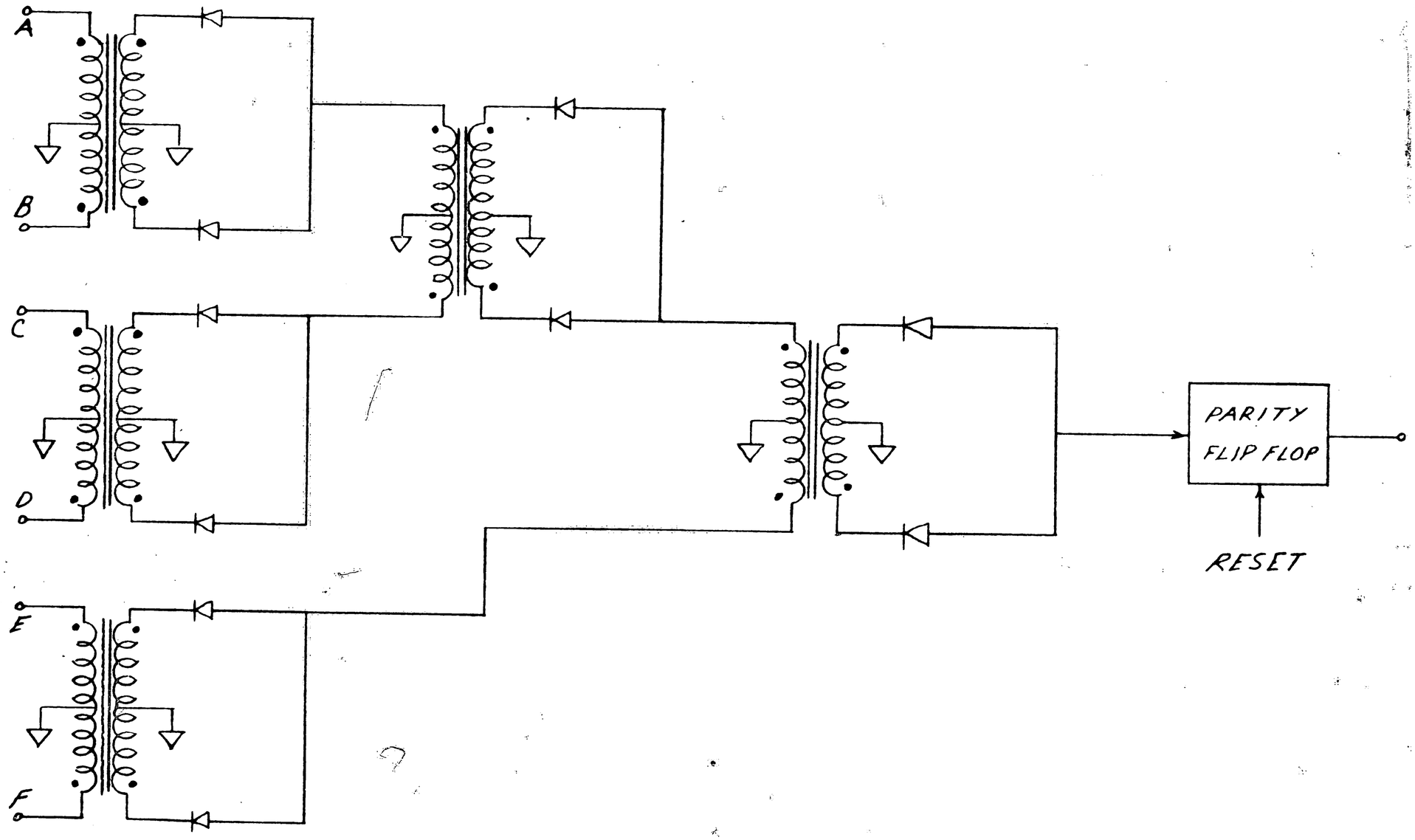

FIGURE 2 - ADD PARITY

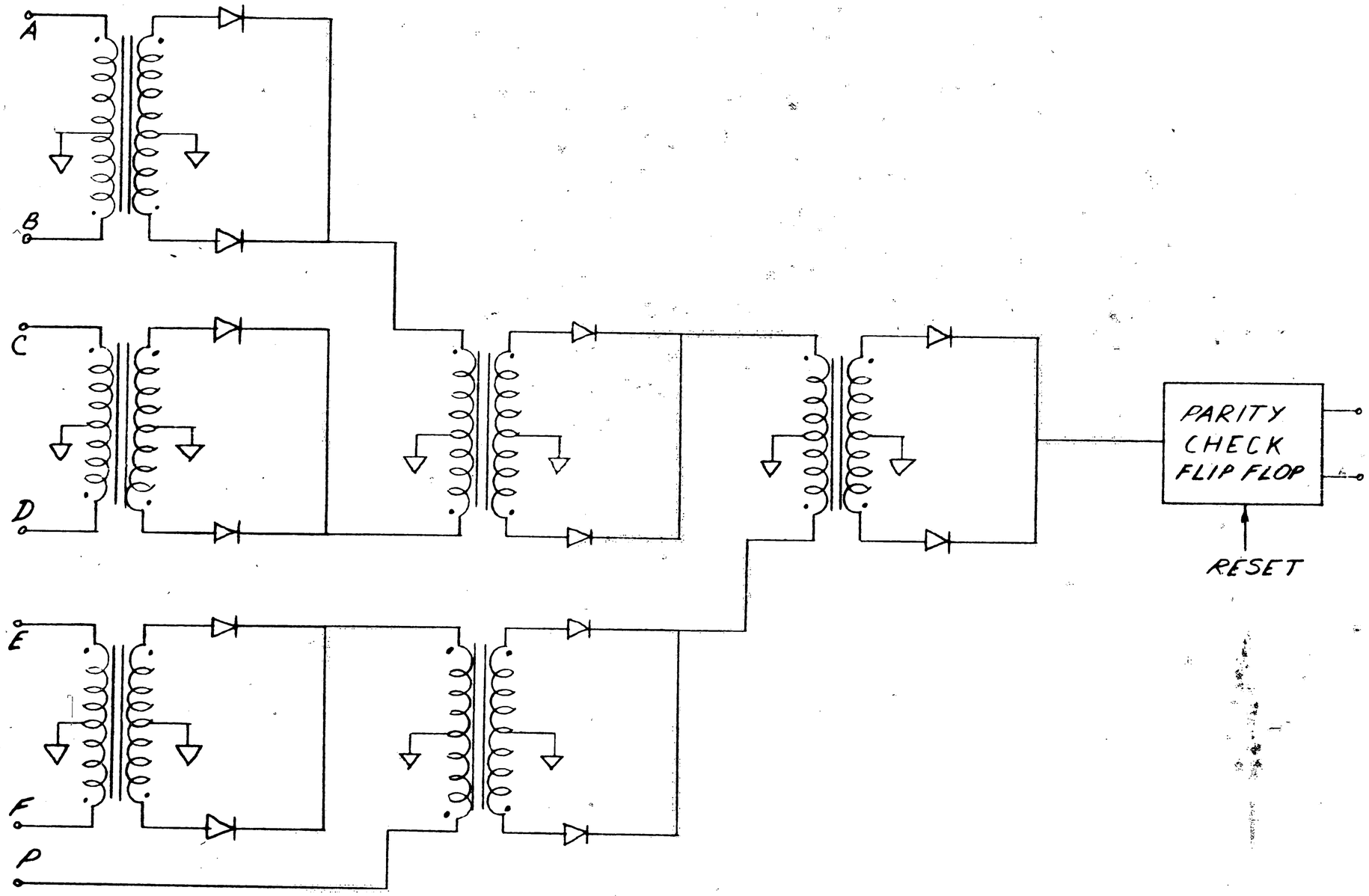

FIGURE 3 - CHECK PARITY

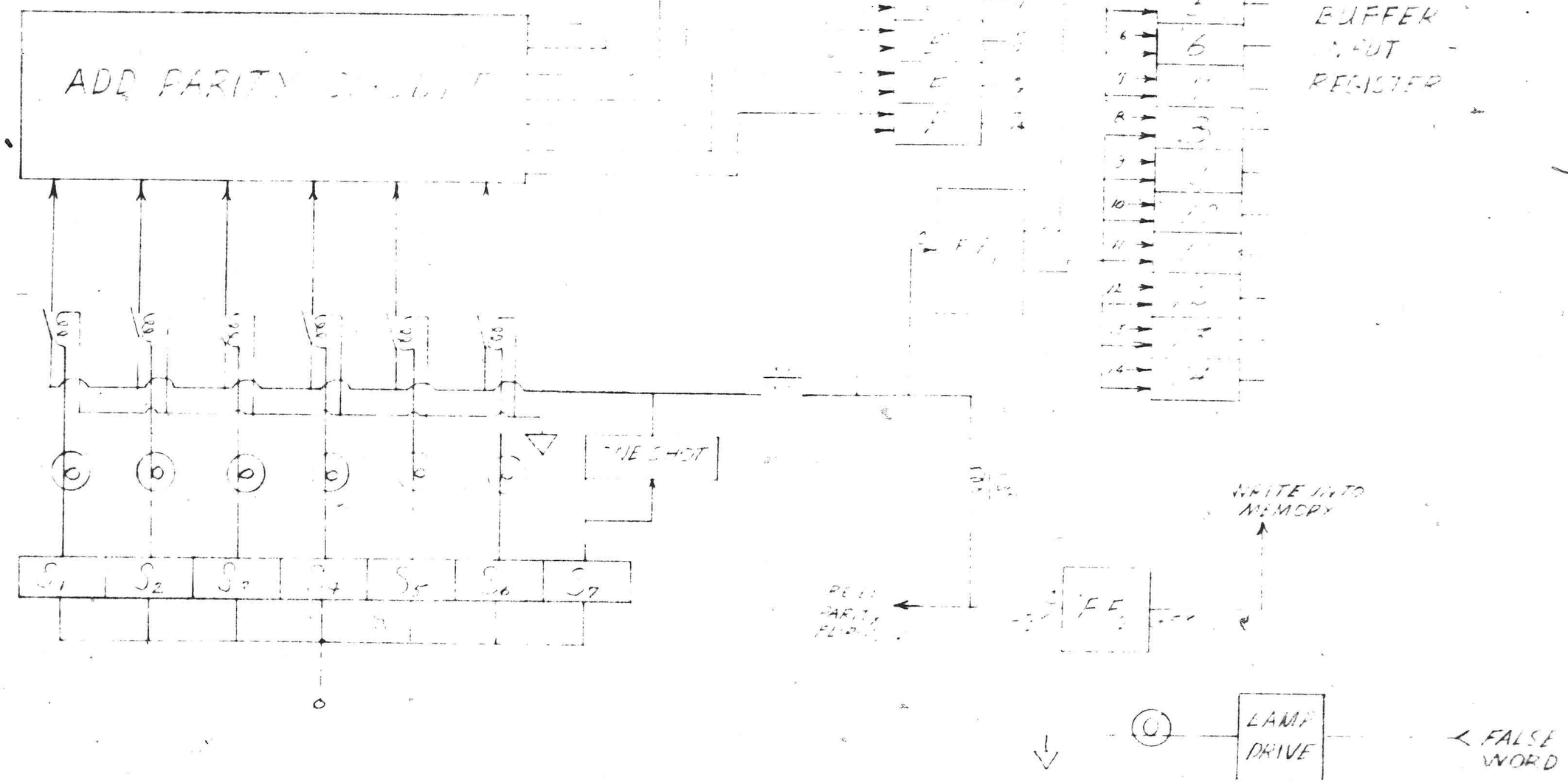

FIGURE 4 — CONSOLE

VITA

Robert L. Billings was born to George and Rita Billings on September 4, 1930, in Pawtucket, Rhode Island. He attended grammar schools in Attleboro, Massachusetts, and was graduated from Attleboro High School in 1948 in that city. He entered the United States Air Force in January, 1951, and was honorably discharged in December, 1954. In February, 1955, he entered the University of Rhode Island to study electrical engineering. During this time he was elected to Tau Beta Pi. After graduation in June, 1958, he began employment at Bell Telephone Laboratories where he is presently employed. He completed the 1960-1961 acedemic year in the Northeastern University Graduate School in electrical engineering and enrolled in the graduate school at Lehigh University in September, 1961.